



INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
				Application Number	10/015,530
				Filing Date	December 12, 2001
				First Named Inventor	Robert T. Plunkett
				Art Unit	2183
				Examiner Name	Aimee Li
				Attorney Docket Number	046301/046000 (QST-046 US)
Sheet	1	of	2		

U.S. PATENT DOCUMENTS					
Examiner Initials ¹	Cite No. ¹	U.S. Patent Document Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US 4,380,046	04-12-1983	Fung	
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Examiner Signature	Date Considered
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Sheet	2	of	2	Attorney Docket Number	046301/046000 (QST-046 US)

U.S. PUBLISHED PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	U.S. Patent Document Number – Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	41.	US 2003/0074473 A1	04-17-2003	Pham et al.	
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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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	47.	Hanna et al., "A Normalized Backpropagation Learning Algorithm for Multilayer Feed-Forward Neural Adaptive Filters," <i>Neural Networks for Signal Processing XI</i> , Proceedings of the 2001 IEEE Signal Processing Society Workshop pp. 63–72 (Sept 2001)	
	48.	Janweijer et al., "A Compact Robin Using the SHarc (CRUSH)," Obtained from: http://www.nikhef.nl/~peterj/Crush/CRUSH-hw.pdf (Sept 1998)	
	49.	Rajagopalan et al., "A Flexible Multiplication Unit for an FPGA Logic Block," <i>Circuits and Systems</i> 4:546–9 (2001)	
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AL/

Examiner Signature	/Aimee Li/	Date Considered	06/11/2009
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